

# FERROELECTRIC NANOTUBES

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**Abstract.** We report the independent invention of ferroelectric nanotubes from groups in several countries. Devices have been made with three different materials: lead zirconate-titanate  $\text{PbZr}_{1-x}\text{Ti}_x\text{O}_3$  (PZT); barium titanate  $\text{BaTiO}_3$ ; and strontium bismuth tantalate  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT). Several different deposition techniques have been used successfully, including misted CSD (chemical solution deposition) and pore wetting. Ferroelectric hysteresis and high optical nonlinearity have been demonstrated. The structures are analyzed via SEM, TEM, XRD, AFM (piezo-mode), and SHG. Applications to trenching in Si dynamic random access memories, ink-jet printers, and photonic devices are discussed. Ferroelectric filled pores as small as 20 nm in diameter have been studied.

## 1. INTRODUCTION

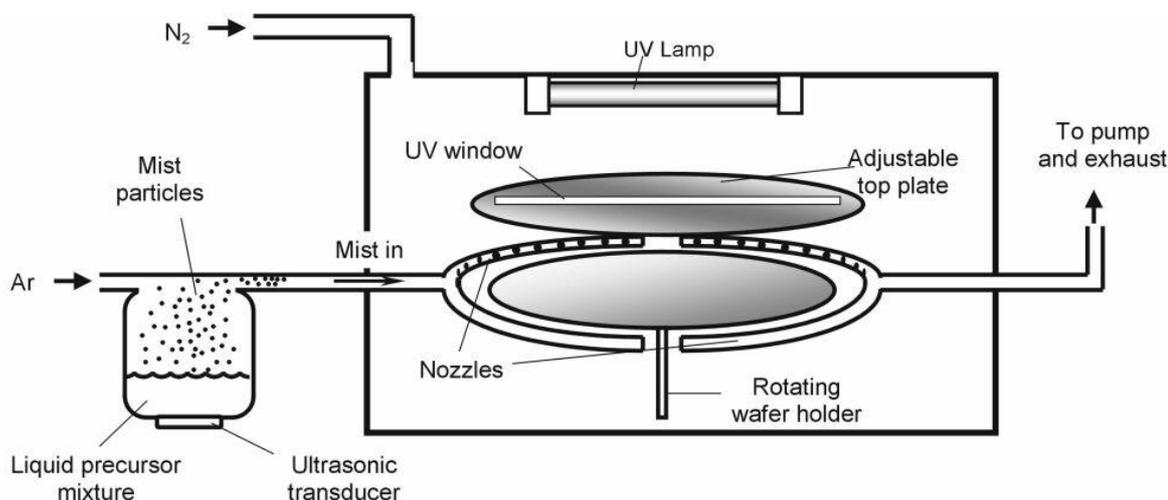
Nanotubes of conducting materials such as carbon have recently received considerable attention. Micro-tubes of nonconducting BN and SiC have also been reported in the patent literature [1-5]. However, ferroelectric nanotubes made of oxide insulators, as reported here, have a variety of applications for pyroelectric detectors, piezoelectric ink-jet printers, and memory capacitors, that cannot be filled by other nanotubes. Hernandez *et al.* demonstrated the fabrication of ferroelectric nanotube bundles from porous alumina substrates [6] and larger ferroelectric micro-tubes have been made previously by sputter deposition about polyester fibres [7-10] – Glen Fox at EPFL has made them [10] from ZnO and PZT, with 23- $\mu\text{m}$  inside diameter. Application advantages of these devices include [10] “enhancing the piezoelectric response

of composite materials by five orders of magnitude in comparison with bulk ceramic materials” and for MEMS. A similar process involving coating rather than filling pores, is given by [7-9], with BN/SiC tubes claimed to be piezoelectric. We report here fabrication of ferroelectric nanotubes of various compositions with structures as small as 20 nm using several techniques. By using porous Si substrates as templates it is also possible to produce regular arrays of discrete nanotubes.

There is a need to deposit uniform coatings of dielectrics on the inside walls of trenches for Gbit Si random-access memories (RAMs), both dynamic DRAMs and non-volatile ferroelectric FRAMs. Thin-film devices, including dielectric capacitors for random-access memories (RAMs) are generally deposited via chemical vapour deposition (CVD), sputtering, or related techniques in which the principal aims are to achieve uniform thickness along the

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**Fig. 1.** Schematic representation of the liquid source misted chemical deposition technique.

inside walls of a high aspect-ratio trench. At present a typical value for the aspect ratio desired is 6 microns deep by 0.1 micron diameter [11]. Here we report such ratios with uniform coatings as thin as 40 nm, these nanotubes can also be used for ultra-small ink-jet printers or for photonic device arrays. The state-of-the-art ink-jet printer (Seiko-Epson) can deliver a 1.0-picoliter droplet and paint a 1.0-micron line for lithography-free printing of integrated circuits [12]; our piezoelectric nanotubes have diameters as small as 0.18 microns, thus suggesting their use for improved nano-ink-jet devices for higher resolution lithography-free IC production.

In the present work we report successful deposition at such aspect ratios of dielectrics such as lead zirconate titanate PZT, barium titanate, and strontium bismuth tantalate (SBT) for ferroelectric RAMs. Diameters can be as small as 0.1 microns, with 40-200 nm wall thicknesses and very deep depths (> 80 nm). This has important implications for Gbit devices and for three-dimensional [3D] integration.

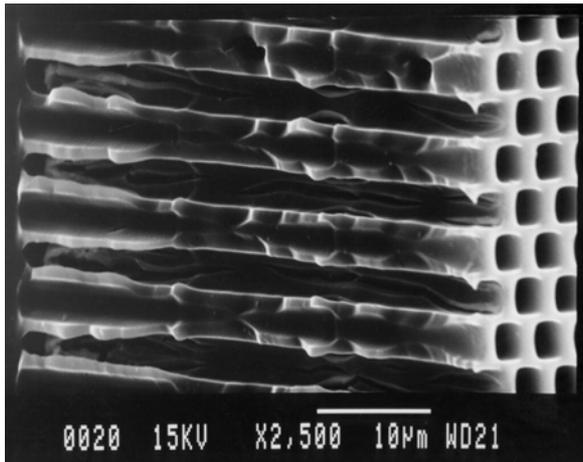
## 2. CHEMICAL SOLUTION DEPOSITION

We report here the use of liquid source misted chemical deposition [13, 14] for filling porous Si substrates. The misted CSD system shown schematically in Fig. 1. The system utilizes a stoichiometrically correct precursor solution that is driven through a multiple-nozzle-type delivery system in close proximity to a rotating Si wafer, which can be simulta-

neously heated, illuminated with ultraviolet light, and/or subjected to d.c. electric fields. The great advantage of this system over sol-gel spin-on deposition is that it achieves excellent step coverage for real commercial devices [13]. Normally it is configured to produce ca. 3-micron droplet diameters, but a 0.2-0.3 micron droplet model is also available [15]. High-speed spin-on rotation for sol-gel precursors would be completely inappropriate for nanotube deposition.

At present, experiments are being carried out to compare misted deposition with pore-wetting. The primary purpose of this comparison is to try to establish whether the electrostatic charges on the droplets play a significant role in the pore-filling, or if the process is driven entirely by surface energy minimization. At the moment, results (using both positive and negative d.c. voltages to the Si substrate) are inconclusive.

During misted deposition is particularly important that each droplet is charged, typically at  $-5e$ , as determined prior studies [15]. The porous Si substrates used in the process are prepared by photo-excitation of majority and minority carriers, concomitant with a wet etch [16, 17]. Using this technique, it is possible to produce regular arrays of pores with diameters ranging from a few hundred nanometers to a few microns, with depths of up to 100 nm. Although not emphasized in the literature, the etching process results, according to our experiments, in a net positive charge for the inside of the Si trenches. Strontium bismuth tantalate was depos-



**Fig. 2.** SEM micrograph of SBT-filled photonic Si substrate indicating deposited material on pore walls.

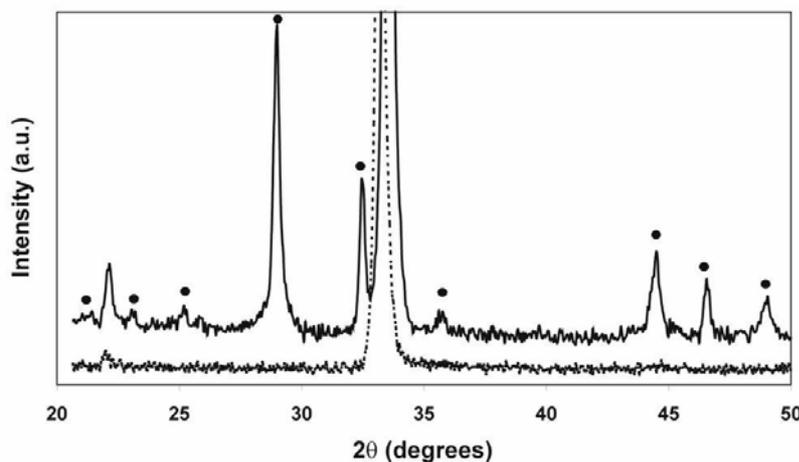
ited on porous Si substrates using a Samco liquid source misted chemical deposition apparatus.

The charged mist droplets produced during the deposition technique behave as in the original Millikan oil drop experiment [18], with the same typical charge of  $-5e$ . Their motion through air at near atmospheric pressure is governed largely by electrostatic forces. The negatively charged ( $-5e$ ) liquid droplets are attracted to the substrate and down the trenches, where they produce remarkably uniform dielectric coatings as thin as 40 nm and as thick as 200 nm, depending upon deposition parameters. We emphasize that this uniformity is not obtainable via conventional CVD or sputtering. The gas phase molecules in CVD deposition are un-

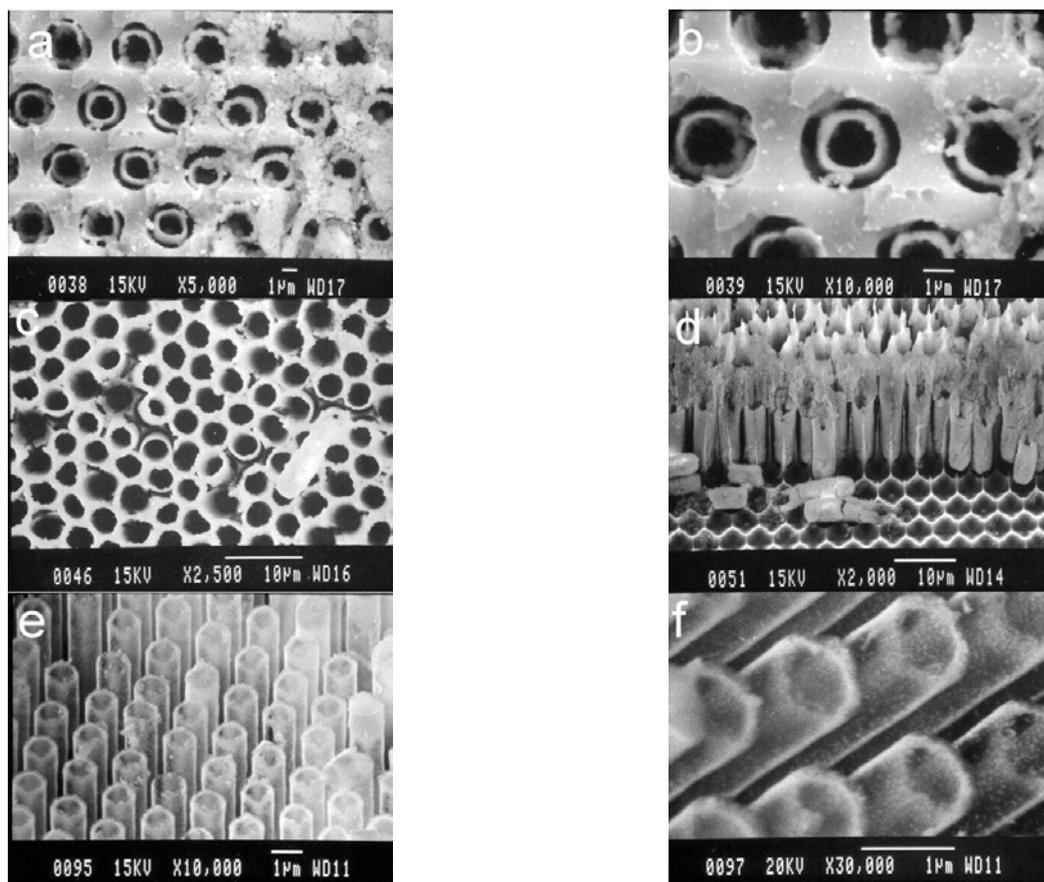
charged, so that the same coating mechanism is completely inoperative for structures with such high aspect ratios, and incomplete penetration of deposited material results in non-uniform coating.

During the deposition process the liquid precursor deposits uniformly on the pore interiors rather than “bottom up” filling [19]. A cross section SEM micrograph, Fig. 2, shows the deposition of material on the pore walls. XRD confirms the formation of the polycrystalline, ferroelectric phase  $\text{Sr}_{0.8}\text{Bi}_{2.2}\text{Ta}_2\text{O}_9$  on the pore interiors after pyrolysis and crystallisation of the precursor, Fig. 3. Afterwards, the surrounding Si substrate can be removed by wet chemical etching, exposing crystalline SBT tubes. A partially filled Si substrate with pore diameter of ca. 2  $\mu\text{m}$  and depth of 80  $\mu\text{m}$  which has been partially filled with SBT is shown in Fig. 4a, b. The Si substrate has been selectively etched for a short time to reveal the SBT tubes, which have a uniform wall thickness of ca. 200 nm.

A second, more porous substrate with larger pore diameters of ca. 3  $\mu\text{m}$  is shown in Fig. 4c, d. The plan view, Fig. 4c, again indicates the uniformity of coating, however, due to the thinness of the Si walls separating the pores, the etching process does not reveal the separated tube structures to the same extent. A cross sectional view after complete removal of the host Si walls between pores is shown in Fig. 4d. This results in a regular array of tubes attached to the host Si matrix only at the tube base. Although these tubes have suffered damage during handling, it is clear that the pores have been filled uniformly to the bottom, a depth of ca 100 $\mu\text{m}$ . This latter structure can be used as a free-standing photonic array. A mostly undamaged array of SBT tubes



**Fig. 3.** XRD of photonic crystal with pore diameter 800 nm, before (---) and after filling (—), indicating the presence of crystalline phase  $\text{Sr}_{0.8}\text{Bi}_{2.2}\text{Ta}_2\text{O}_{9+g}$  (•).



**Fig. 4.** SEM micrograph indicating a plan view of a regular array of SBT tubes in host silicon substrate (a) with diameter ca. 2  $\mu\text{m}$  and wall thickness ca. 200 nm (b). Larger diameter SBT tubes in plan view (c) and cross sectional view of free standing tubular array (d). Nanotube array with tube diameter ca. 800 nm (e) and wall thickness < 100 nm (f).

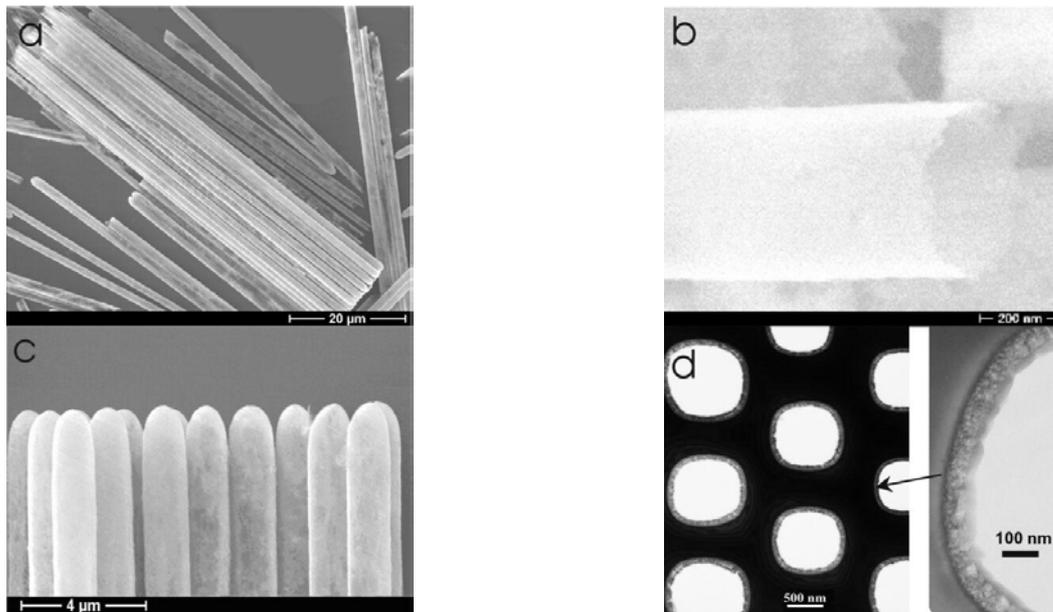
of diameter ca. 800 nm is shown in Fig. 4e. The tubes are very uniform in dimension with wall thickness < 100 nm, Fig. 4f, and are perfectly registered over several mm.

### 3. POLYMERIC WETTING

The approach consists of wetting of the pore wall of porous templates, either porous alumina or macroporous silicon, by a polymeric precursor containing the metals in the stoichiometric quantities. Lead zirconate titanate ( $\text{PbZr}_{0.52}\text{Ti}_{0.48}\text{O}_3$ ) and barium titanate ( $\text{BaTiO}_3$ ) nanotubes were fabricated by infiltrating at room temperature a previously fabricated template [20] by simply bringing in contact the metalorganic precursors and the template. Within a few minutes a thin precursor uniform layer forms on the pore walls from the top down to the bottom of the pores by capillary action. Further investigations showed that the wetting process is so uniform that

always a complete covering of the whole surface of the pore walls occurs. As it was shown for several polymers, the driving force of the wetting process is the reduction of the surface energy [21,22]. Oxide tubes of the appropriate ferroelectric perovskite phase are obtained by thermal annealing and crystallisation.

Free ferroelectric tubes can be easily obtained by selective etching of the silicon template. Fig. 5a shows straight and smooth  $\text{BaTiO}_3$  hollow nanotubes with a diameter of about one micron, length of about 50  $\mu\text{m}$  and a wall thickness of 70 nm. The outer diameter can be easily tuned by using different templates. Using nanoporous alumina template the diameter can range from 50 nm to about 400 nm, while using mesoporous silicon it can vary from 400 nm up to several micrometers [16]. The tube length depends on the pore depths and it can be from few micrometers up to more than 100 mm. As shown in Fig. 5b, a single coating produces a tube wall as



**Fig. 5.** SEM image of (a) a bundle of free  $\text{BaTiO}_3$  tubes, (b) of an opening end, and (c) of capped tip of  $\text{BaTiO}_3$  nanotubes. (d) Cross-section transmission electron microscopy images of PZT nanotubes in silicon template.

thin as 50 nm. Increase of the wall thickness is easily achieved by repeated infiltration followed by a low temperature annealing and after the final infiltration the tubes are crystallized by the high temperature annealing. TEM analysis (Fig. 5d) shows that the as deposited and crystallized tubes of both  $\text{BaTiO}_3$  and PZT show a tube wall consisting of a crystalline layer sandwiched between two amorphous layers at the silicon-ferroelectric interface and at the internal surface.

#### 4. SOL-GEL DIPPING

For ultra-small (20-30 nm) nano-rods and nano-tubes PZT was embedded into porous silicon and alumina matrices by dipping into a precursor (for 3 hours) prepared by a sol-gel method followed by crystallization during thermal annealing. Deposition of sol on the pore walls proceeds as a result of adsorption of the sol particles (micelles are positively charged) to membrane pore walls [23]. Short immersion times should provide tubules, while longer times yield fibres [24] (depending on pore size, concentration, surface tension, shrinkage, etc.). The structure of porous substrates as well as PZT nanostructure was studied by AFM and TEM. It was found that on top of the porous Si nanostructure a PZT layer is formed after dipping. In order to remove the PZT film the surface was either etched by argon beam (for sili-

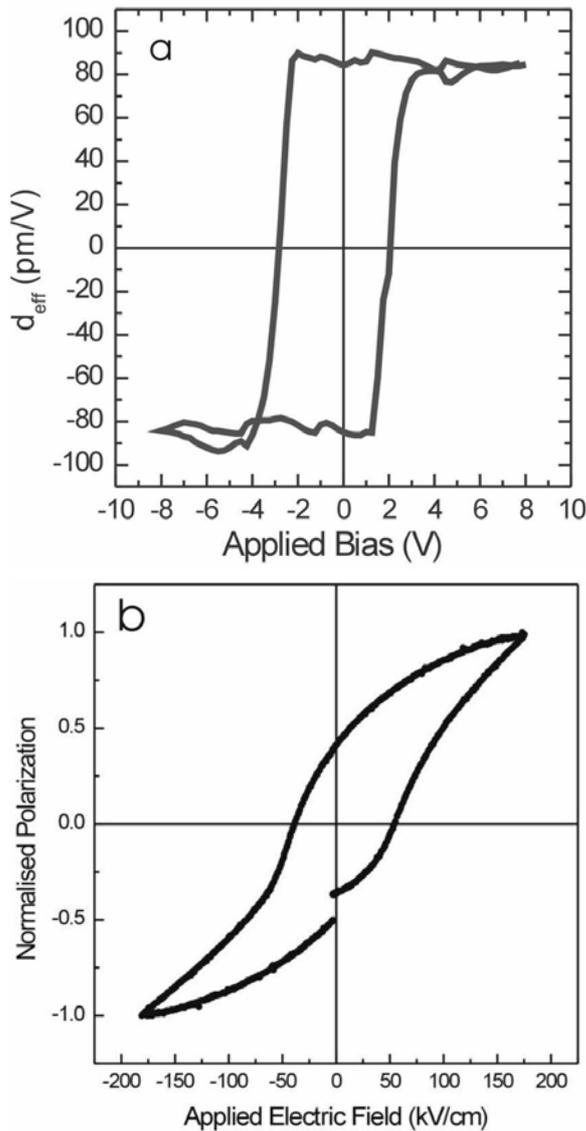
con substrate) or cleaned by the solvent rinsing prior to annealing (alumina substrate).

#### 5. PROCESSING DETAILS

Liquid precursor (from Inorgtech) for chemical solution deposition consisted of a 0.1 M solution of Sr-, Bi-, Ta-ethylhexanoates in toluene, with appropriate ratios of Sr, Bi and Ta to give the resulting stoichiometry  $\text{Sr}_{0.8}\text{Bi}_{2.2}\text{Ta}_2\text{O}_9$ . PZT 9906 Polymer and BATIO 9101 Polymer (Chemat Technology) were used for pore wetting. PZT sol-gel precursor was prepared via anodic dissolution of Ti-Zr in  $\text{CH}_3\text{OC}_2\text{H}_4\text{OH}$  and dehydration of  $\text{Pb}(\text{CH}_3\text{COO})_2 \cdot 3\text{H}_2\text{O}$  with  $(\text{CH}_3\text{CO})_2\text{O}$ . Crystallisation by thermal annealing was carried out in air at 650-700 °C (30 mins, PZT), 850 °C (1 hr, SBT and  $\text{BaTiO}_3$ ). Wet etching was carried out in an aqueous solutions of 15 vol% HF / 50 vol%  $\text{HNO}_3$  or 20 wt % KOH solution at 90 °C.

#### 6. HYSTERESIS

In order to measure the piezoelectric and ferroelectric properties, free standing PZT and  $\text{BaTiO}_3$  nanotubes were prepared, deposited onto platinum-coated silicon wafer, and subsequently annealed one hour in oxygen at 700 °C [25]. The ferroelectric properties were measured using scanning force micros-



**Fig. 6.** Piezoelectric hysteresis loop of an individual PZT tube measured by piezoresponse AFM (a). Hysteresis loop of a flat SBT film made in an identical manner to the SBT nanotubes (b).

copy in the so-called piezoresponse mode [26,27]. Individual tubes were probed by a conductive tip and characterized by measuring the local piezoelectric hysteresis. Fig. 6a shows the piezoelectric hysteresis loop obtained on a PZT tube with an outer diameter of 700 nm and wall thickness of 90 nm. The piezoelectric signal is an unambiguous proof the piezoelectricity of the tubes and the hysteresis in the piezoresponse signal is directly associated with the polarization switching and ferroelectric properties of the sample. Moreover, the rectangular shape of the hysteresis loop showing a sharp ferroelectric switching at a coercive voltage of about 2 V is connected with a high quality of ferroelectric material.

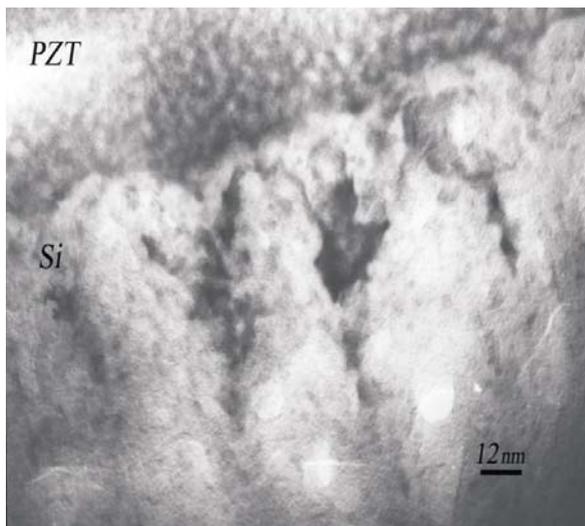
The effective remanent piezoelectric coefficient is of about 90 pm/V and is comparable with usual values obtained on PZT thin films.

Here we point out that it is difficult to compare the above values to the piezoelectric coefficients of bulk material since the measurement was performed on a tube geometry which has a relatively complicated field distribution and vibrational modes; however, the suggested inference is that the polar axis lies primarily along the nanotube and not through its walls, since the effective  $d$ -value is ca. 10% of the expected value for an oriented film.

For the SBT array, it was not possible to apply electrodes in the same way for electrical characterisation, however a flat SBT film deposited and annealed under the exact same conditions as used to produce the array shown in Fig. 4e,f showed good FE hysteretic properties, Fig. 6b. The coercive field,  $E_c$  (determined as the average of positive and reverse coercive fields) was ca. 46 kV/cm. As yet, we have not applied concentric electrodes to the tubes (that is, with cathode inside the cylindrical tubes and anode outside). The hysteresis data for PZT tubes shown in Fig. 6a were obtained by laying individual tubes down on a metal ground plate, sputtering semicircular top electrodes from above, and measuring the switching across a small arc of the tube circumference. However, a greatly superior device would have concentric cylindrical electroding, and Steinhart et al. recently used porous anodic alumina templates to grow palladium nanotubes [29]. Using a similar method we hope to alternately deposit Pd or Pt and SBT to produce a concentric electrode/FE/electrode structure in each nanotube. The use of the photonic crystal template with a regular array of pores has significant benefits over other porous substrates in that the coatings/tubes produced are also in a registered array ordered over several mm's or even cm's. This facilitates addressing of such an array for device applications.

## 7. ULTRA-SMALL (20 nm) DEVICES

The shape of the nanotubes depends on the quality of a matrix. In porous silicon the decrease of the pore size down to 10 nm leads to a deterioration of the pore shape and its deviation from cylindrical, Fig. 7. Simultaneously, it becomes much more difficult for the precursor to penetrate the pore. Additionally, a thick (>100 nm) PZT film is formed on top of the structure during a dipping, which should be removed by argon beam etching. The thickness of a residual on-top PZT film does not exceed 5 nm and the maximum PZT penetration depth is about



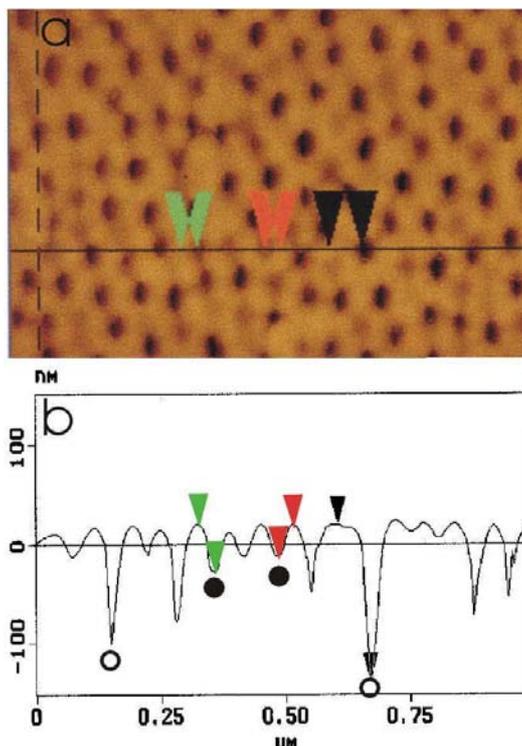
**Fig. 7.** Bright field TEM of PZT filled porous Si substrate indicating the irregular pores filled with PZT and PZT surface film.

30 nm. Therefore, for very small pored silicon substrates, nanoparticles rather than nanotube structures are formed.

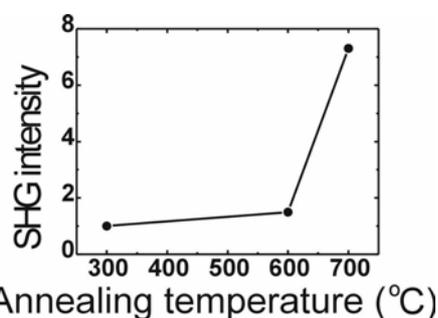
Alumina membranes with 20-30 nm pores with high aspect ratio and perfect cylindrical shape can be obtained by an electrochemical etching [30]. Since the surface of the pore is smooth, and no constriction along the pore appear, penetration depth of a precursor is higher and may reach 100 nm. For PZT/alumina structures, the top film is also formed but can be removed by dipping in a solvent. Fig. 8 shows the top AFM image of the PZT/alumina nanostructure (a) and the crosssectional view (b). After the rinsing in a solvent the very top PZT layer is removed not only from the surface, but also from the top of the pores. As a result, a shallow hollow (<10 nm) at the top of each pore is observed. Deep hollows (100 nm) exist for pores in which PZT precursor does not penetrate at all. Therefore, for an alumina substrate, a nanotube ferroelectric structure is formed.

## 8. SECOND HARMONIC GENERATION (SHG)

Optical second harmonic generation (SHG) was used to distinguish between paraelectric and ferroelectric phases of PZT nanolayers embedded in silicon and alumina membranes. These SHG measurements were performed with the use of a 100-fs Ti: sapphire amplified laser at the fundamental wavelength of 800 nm and with a femtosecond optical parametric amplifier at the fundamental wavelength



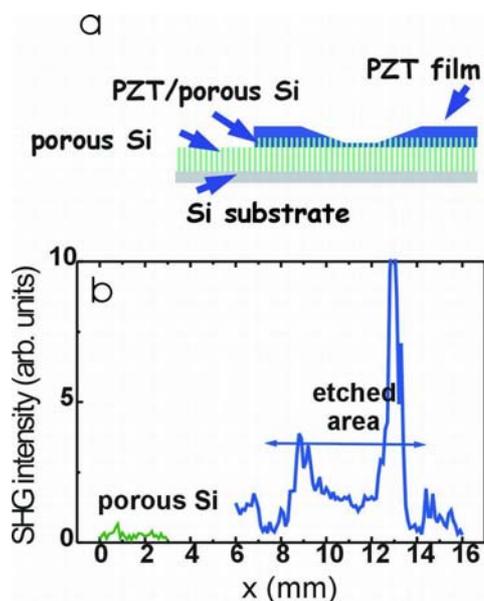
**Fig. 8.** AFM image of PZT nanostructure embedded into porous alumina (a) and probe signal in cross section (b) indicating filled (•) and empty (o) pores.



**Fig. 9.** SHG intensity as a function of annealing temperature for PZT filled porous Si.

in the range of 670-520 nm. The repetition rate was 1 kHz, pulse energy 0.05 mJ, the spot diameter 100  $\mu\text{m}$ . The SHG radiation was detected by a PMT and a lock-in amplifier after filtering by monochromator and colour filters.

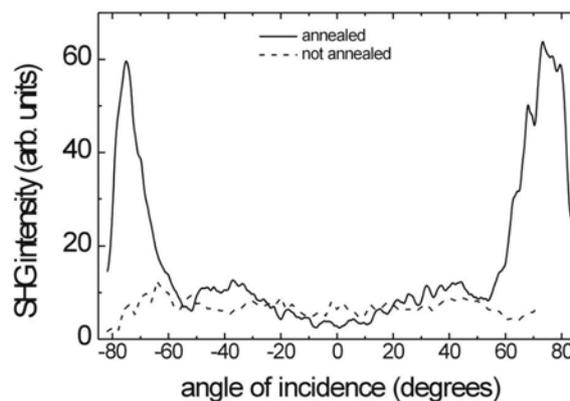
Application of these method is based on the difference in the symmetry of the phases: paraelectric phases are centrosymmetric and do not produce SHG in the bulk of the material, while ferroelectric phase is non-centrosymmetric and produce a very strong SHG signal. For both PZT/Si and PZT/alumina the SHG intensity was increased by more than order of magnitude after annealing above 600  $^{\circ}\text{C}$ , Fig. 9, confirming formation of the ferroelectric state in PZT nanoclusters after annealing.



**Fig. 10.** Model of the PZT/porous Si structure after etching (a) and SHG intensity along the etched area and porous membrane (b).

SHG of a PZT/Si nanostructure measured in the reflection geometry at 45 degrees angle of incidence is shown in Fig. 10. The laser beam was scanned along the area etched by the argon beam. Fig. 10a shows the model of the etched area and the SHG intensity during scanning. The silicon membrane produces small SHG signal whereas the SHG intensity from the film is about the order of magnitude higher, Fig. 10b. Decreasing the film thickness leads to the decrease of the SHG intensity following by a sharp peak corresponding to the film/nanostructure interface region. Further etching of a nanostructure reduces the signal gradually. A sharp increase of the SHG intensity on top of the PZT/Si nanostructure may arise due to change of the boundary conditions for the ferroelectric particles and due to interference effects as well.

For PZT/alumina nanostructure SHG intensity was measured in the transmission geometry as the function of angle of incidence, Fig. 11. This geometry allows to emphasize the influence of the shape of the nanoparticle. The measurements were carried out before and after annealing. The increase of the SHG intensity of *ca.* one order of magnitude indicates the phase transition into ferroelectric state during annealing. The strong maxima for incidence angle about 85 degrees point to an appearance of a strong local field that may be due to the column-like structure of the particles.



**Fig. 11.** Angular dependence of SHG intensity for PZT filled porous alumina.

## 9. SUMMARY AND APPLICATIONS

Using porous photonic Si crystals with a regular array of pores or diameter 400 nm to a few microns and 100 nm deep as templates, we have successfully produced uniform coatings of FE <100 nm thick with high aspect ratios. These coatings have potential application in DRAM and FRAM devices. On partial removal of the Si template, it is possible to produce a periodic array of nanotubes in which each tube is completely discrete. This is in contrast to other template approaches, which produce either individual, free-standing nanotubes or "bundled" entangled structures. The formation of a periodic array has several advantages in terms of addressing/registration for device applications, for which design issues of importance include electrode configuration, "cross-talk" and the possible requirements of pass-gate transistor isolation of each nanodevice.

Just as various applications of carbon nanotubes have been investigated, it is envisioned that nanotubes made from functional oxides can be used in fluidic devices for analysis and control of molecular species, nanoelectronic devices, catalysis, and nanoscale delivery vehicles. The very large surface/volume ratio makes catalytic devices particularly attractive. Piezo- and ferroelectric nanotubes therefore have potential for a variety of applications in addition to ferroelectric memory devices. With further etching it is possible to break the mechanical bond between the tubes and substrate producing free standing tubes. These tubes may also have interesting potential applications including piezoelectric syringes for drug delivery implants (triggered

externally by rf or other stimuli). In addition to the application in Si DRAM trenching, these processes may allow fabrication of devices for mass storage analogous to the IBM millipede (30), and tunable [2D] photonics.

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