Rev.Adv.Mater.Sci. 8 (2004) 176-184

FORMATION OF CONTACTS AND INTEGRATION WITH SHALLOW JUNCTIONS USING DIBORIDES OF Ti, Zr AND Hf

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Received: December 15, 2004

Abstract. Metallic diborides TiB_2, ZrB_2 and HfB_2 were used for the formation of contacts integrated with ultra shallow junctions required in deep submicron devices in integrated circuits. The films were deposited by electron-beam evaporation on an oxide free surface of both p- and n-type Si. Rapid thermal processing (RTP) in N_2 ambient was performed using temperatures up to 1100 °C and time up to 30 s. Electrical characterization of the films was done using sheet resistance measurements, which show decreasing resistance with increasing thermal budget of the annealing processes. Test structures on p-type Si were fabricated to determine contact resistance before and after the annealing processes. The borides form ohmic contacts on p-type Si after deposition and improve their ohmic behavior after annealing; specific contact resistivity decreases with temperature. On n-type Si, the formation of Schottky diodes was determined by current-voltage (I-V) and capacitance-voltage (C-V) measurements for as deposited and annealed structures.
A set of complementary material testing including X-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS), cross-section transmission electron microscopy (TEM), and Rutherford Backscattering (RBS) was done to determine stoichiometry, composition, and crystallographic structure of the processed films. All boride films showed recrystallization, which increases with thermal budget of the annealing processes, as identified by XRD and by TEM with electron diffraction. Material studies show very high thermal stability of the diborides if their composition is stoichiometric. However, this stability deteriorates in nonstoichiometric layers, which leads to larger than desired B outdiffusion clearly detected by SIMS results.

1. BACKGROUND AND MOTIVATION

CMOS devices scaled down to deep 0.1 μm dimensions [1,2] require ultra shallow junction depths in the source and drain (S/D) regions with abrupt dopant profiles. The International Roadmap for Semiconductors (ITRS) predicts aggressive scaling of the junction down to 13.8 nm in 2007. Such very shallow junctions lead to parasitic resistances in metal oxide semiconductor field effect transistors (MOSFET), which have to be alleviated by using high surface concentrations [3]. However, difficulty in realization of such a schemes prompted theoretical verification of the posted requirements [4]. It now became more evident that it is in fact possible to relax these stringent needs for the profile abruptness from 0.5 nm/dec to 2 nm/dec and face only small penalty of a 1% degradation of I_{on} at fixed I_{off}. In addition, the larger profiles' abruptness leads to degradation of the V_T roll-off and increased drain in-

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duced barrier lowering (DIBL) due to charge sharing [5].

Fabrication of very steep ultra shallow and highly doped junctions is difficult due to enhanced diffusion (transient enhanced diffusion TED [6] and B enhanced diffusion BED [7]) and low dopant activation (down to 25% [8]) even for flash [9] or laser annealing [10]. Requirements for low resistive and extremely shallow S/D regions call for more conductive materials than even highly doped silicon. Such candidates include SiGe alloys [11-14] which show significantly reduced electrical resistivity (ρ_{min}=300 μΩcm) and contact resistance as low as $1.5 \cdot 10^{-8}$ Ωcm^2. It appears that the challenges of junction fabrication will be alleviated in SOI [15] devices because junctions will be controlled by the Si thickness. Another currently available solution is silicon on nothing (SON) [16,17] where shallow doping is confined to the thin Si layer or is limited by dielectric pockets [18] also efficiently improves device operation.

Formation of contacts [19] is another fabrication challenge to ensure small contact resistance and low leakage currents, which can be degraded by silicon consumption during silicidation of shallow junctions. Even with monosilicides contacts such as NiSi, further device scaling will require elevated S/D regions for lowering parasitic resistances [20] and for making shallow junctions immune to short channel effects (SCE). In the near future, contact resistance R_{co}, will dominate total parasitic resistance [21,22] and its role in device degradation will increase with device scaling. At the 70 nm node, 70% of the resistance will come from the contact resistance rather than from the accumulation resistance of the S/D regions. Since contact resistance decreases with lowering barrier heights and increasing dopant concentrations at the interface, it appears that SiGe, due to its smaller energy bandgap compared to Si can effectively decrease contact resistance via reduced barrier heights. However, process integration issues of shallow junction and contact formation by silicidation are also difficult [23].

Another option comes from the revived concept of Schottky contacts used in the S/D regions [24] with much smaller parasitic resistances, proposed to improve scaling down devices to 27 nm channel length [25]. However, it is still hindered by technological difficulties related to low barriers materials required for contact formation in P- and NMOS transistors and low leakage currents [26-28].

In this work we tested the possibility of implementation diborides of transition metals for contact formation and/or their integration with ultra shallow junctions. They have the lowest bulk resistivity values of all borides i.e. TiB_2 9-15 μΩcm, ZrB_2 7-10 μΩcm and HfB_2 10-12 μΩcm (isomorphous with TiB_2 and ZrB_2). However, for thin films these values are usually larger since both the crystallographic structure including grain size and porosity, stoichiometry and contaminants (such as oxygen incorporated during some deposition processes) affect the electrical conductivity. The lowest resistivity values of thin films after annealing found in the literature are 36 μΩcm for TiB_2 [29] and 25 μΩcm for ZrB_2 [30] but larger values 500 μΩcm for TiB_2 or 250 μΩcm for ZrB_2 were also reported. Selection of these borides is also based on their thermodynamic stability that will limit outdiffusion of boron during thermal annealing therefore ensuring formation of ultra shallow junctions with very high surface concentrations, which are necessary in ohmic contact formation. On the other hand, with smaller or no B outdiffusion, Schottky barriers will be formed, which would have low leakage currents due to thermal stability of the compounds that would not degrade the interface roughness. The stability of stoichiometric TiB_2 films has been shown up to 1092 °C [31] .

2. EXPERIMENTAL PROCEDURES

We used low doped (100) Si epitaxial wafers both p-type and n-type. They were cleaned using (old) IMEC clean H_2SO_4: H_2O_2 (4:1), DI rinse, and HF (0.5%) and 0.1% IPA in DI water. Alternatively, we also used vapor HF etching (1:10 HF in H_2O) for 60 sec prior to the deposition process. Electron beam evaporation at 8 keV was used for deposition of all boride layers from melted chunks of TiB_2, ZrB_2, and HfB_2. Base pressure was in the range of high $1 \cdot 10^{-5}$ Pa and the deposition pressure did not exceed $2.5 \cdot 10^{-4}$ Pa. The deposited films were from 20 to 100 nm thick with or without a 5 nm Si capping layer deposited in-situ by e-beam for oxidation protection during annealing. Test structures were patterned using photolithography with wet etching for the film removal. TiB_2 was etched in H_2O_2, while HfB_2 and ZrB_2 were etched in H_2O_2 with 5% HF. Rapid thermal processing was performed on patterned and unpatterned films in the same RTP runs in an N_2 ambient. We used temperatures of 700-1100 °C for 1-10 sec. Electrical characterization included measurements of test structures by I-V and C-V in reverse and forward directions as well as sheet resistance. We analyzed formation of ohmic contacts using p-type patterned wafers with various dot sizes. Diode structures were tested using n-type wafers to

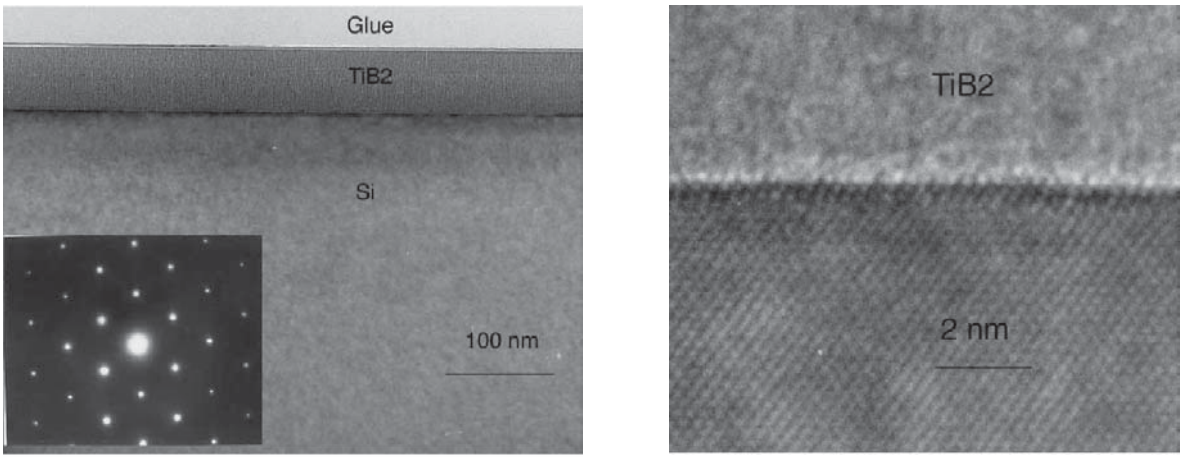

Fig. 1. TEM micrographs of a deposited TiB_2 layer with diffraction pattern: low resolution (a), and high resolution (b).

monitor changes in Schottky contact properties as a function of annealing conditions and/or subsequent formation of p-n junctions.

Various characterization steps such as XPS, RBS, TEM, SIMS, and XRD were performed on selected samples to assess information related to possible changes in boride composition, structure, and dopant outdiffusion as well as to monitor oxidation susceptibility.

3. RESULTS AND DISCUSSION

The deposited films of diborides were tested before and after annealing to verify film uniformity and composition including contamination by oxygen, which otherwise would deteriorate resistivity. Deposited thin films of diborides were uniform in thickness and their structure was amorphous as confirmed by cross section TEM micrographs with small size diffraction patterns (Fig. 1). Cleaning steps used prior deposition as well as evaporation conditions of these high melting point materials did not degrade interface quality. From the XPS and RBS results, we conclude that the films were uniformly stoichiometric. Fig. 2 shows RBS spectra of TiB_2 both after e-beam deposition and subsequent annealing in RTP at high temperatures. Very similar RBS results were

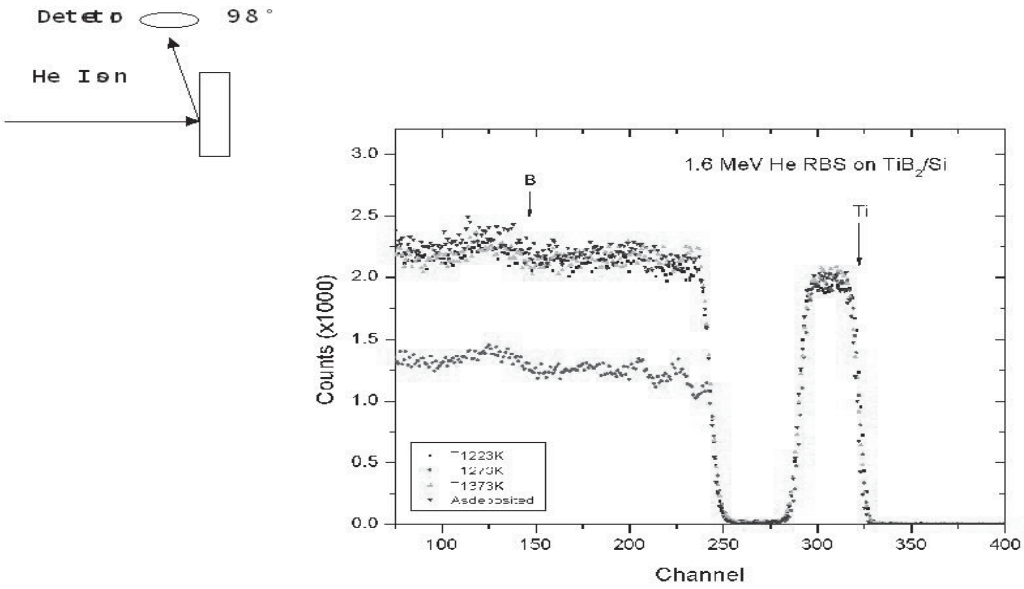

Fig. 2. RBS spectra of TiB_2 layers after deposition and after RTP annealing at various temperatures: 950 °C, 1000 °C, and 1100 °C.

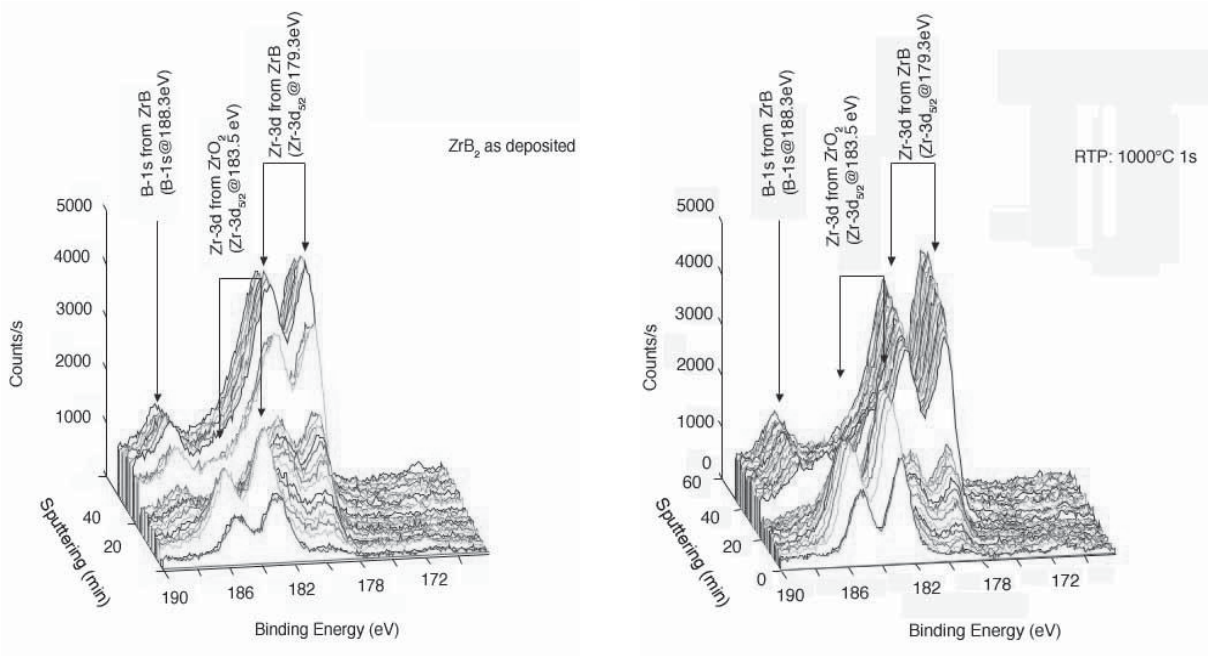

Fig. 3. XPS spectra for ZrB_2 as deposited, (a) and annealed at 1000 °C for 1s, (b).

obtained also for ZrB_2 and stoichiometric HfB_2 (not shown here) confirming high thermodynamic stability of diborides in an oxygen free ambient. An important aspect of such stability for device application is an improved surface roughness at the contact interface with Si compared to the silicide/Si interface, which due to roughness, could increase leakage currents and/or affect energy barrier heights as well as their homogeneity. On the other hand, its drawback is that a nonintimate contact can be formed with an interfacial layer that would change the barrier height and ideality coefficient *n*. Oxygen contamination, which was observed in XPS analyzes in deposited and annealed films was limited only to the surface of the films as shown for ZrB_2 in Fig. 3 while bulk of the film showed unchanged composition. Similar behavior was observed for TiB_2 (Fig. 4) where RTP annealing, even at high temperatures did not change the stoichiometry or thickness of the films recorded by XPS. Within resolution limits of XPS we did not detect silicide formation at the silicon surface. Despite higher susceptibility to oxygen degradation in TiB_2 than in ZrB_2, formation of B and Ti oxides was identified also only at the surface layer (Fig. 5). A thin silicon cap deposited on the boride layer effectively would prevent oxygen incorporation.

Electrical measurements done for all borides deposited on n- and p-type silicon with epi- layers and annealed at various RTP conditions included I-V and C-V characteristics. Fig. 6 shows formation of ohmic contacts with resistance decreasing with temperature and time of RTP. Sheet resistance, which decreases up to 3 times after RTP annealing (down to 50 $\mu\Omega$cm for TiB_2), is partly credited for the improvement such ohmic behavior. It can be linked to film recrystallization since increasing grain growth improves properties of carrier transport. Recrystallization was clearly detected in all our films with the grain size correlated both with the annealing and deposition conditions. Small size diffraction patterns (DP) identified polycrystalline growths of TiB_2, ZrB_2, and HfB_2 in respective films. We did not detect (DP) silicides even for the largest thermal budget processes.

The corresponding specific contact resistance obtained after annealing of borides on p-type Si with test structures made of dots of six different sizes resulted in the R_c values decreasing down to $2 \cdot 10^{-6}$ Ωcm^2 with increasing thermal budget of RTP. Since contact resistance depends both on barrier height and dopant concentrations at the M/S interface, if R_c changes one could expect a metal work function change and increased [32] concentration of B due to outdiffusion. Work function changes can occur due to recrystallization, which causes a well-documented crystal orientation effect. On the other hand, B outdiffusion was found to be quite small (if any)

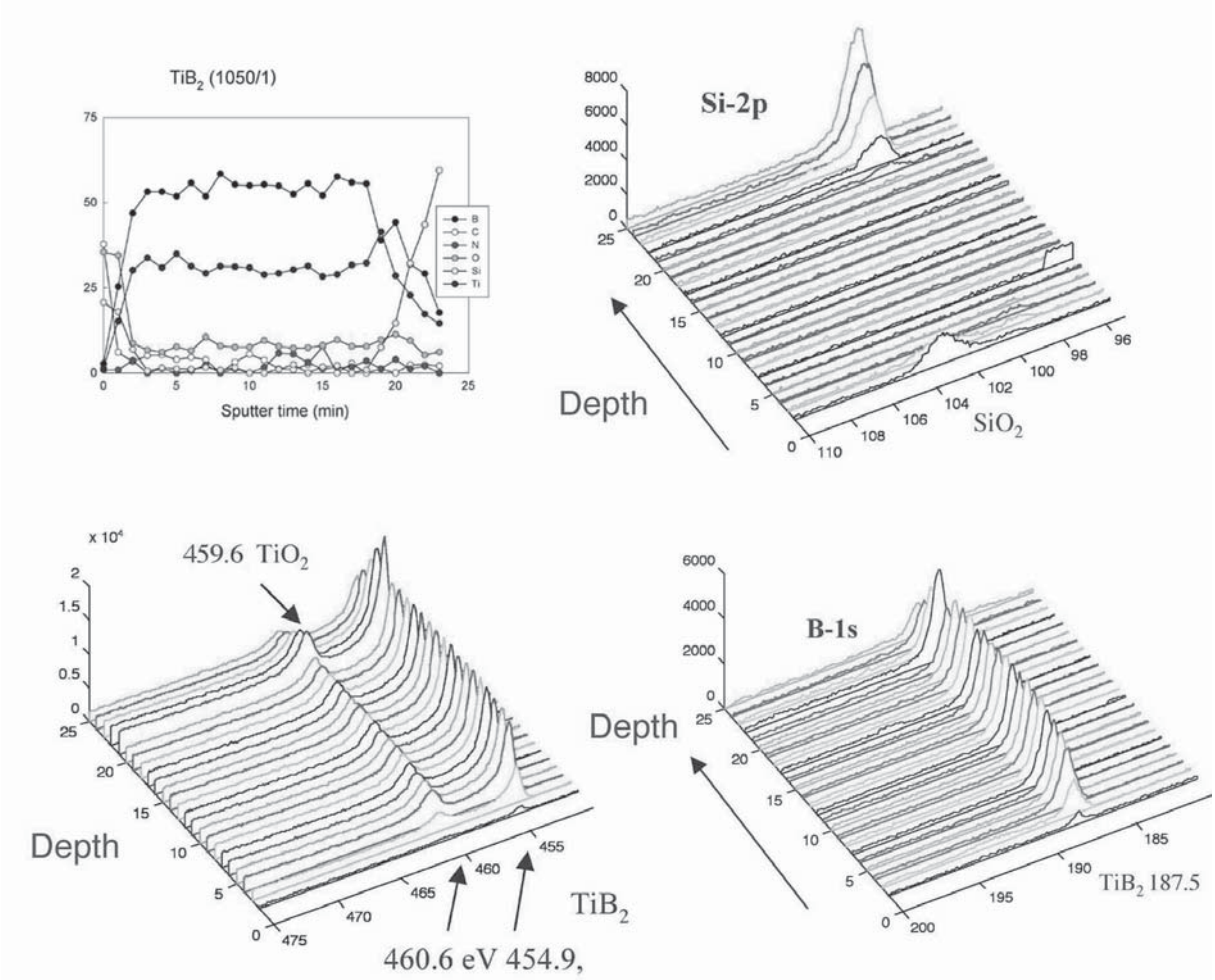

Fig. 4. XPS spectra with depth profiling of TiB_2 layer annealed at 1050 °C for 1 sec. Spectra of constituent elements B, Ti as well as Si are also profiled in the films.

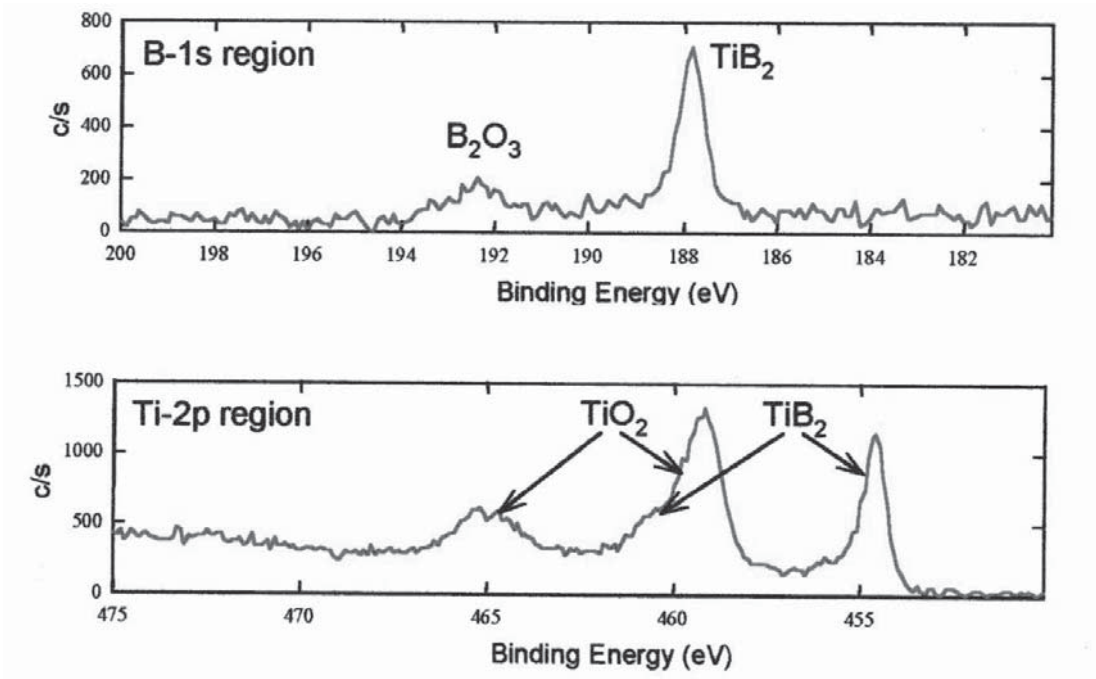

Fig. 5. XPS spectra obtained for the surface layer of the TiB_2 film annealed at 1050 °C for 1s show formation of both boron oxide and titanium oxide.

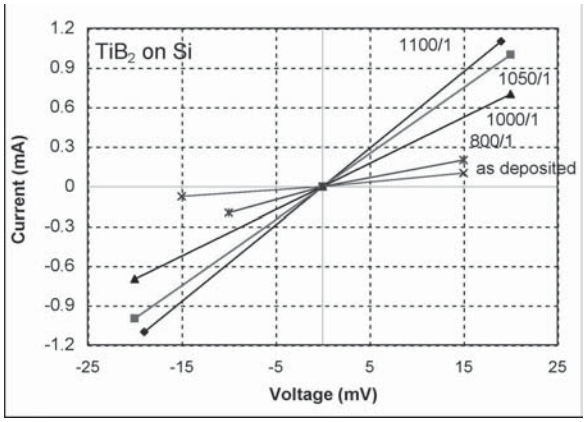

Fig. 6. I-V characteristics for TiB_2 contacts on p-type Si annealed at various thermal conditions of RTP.

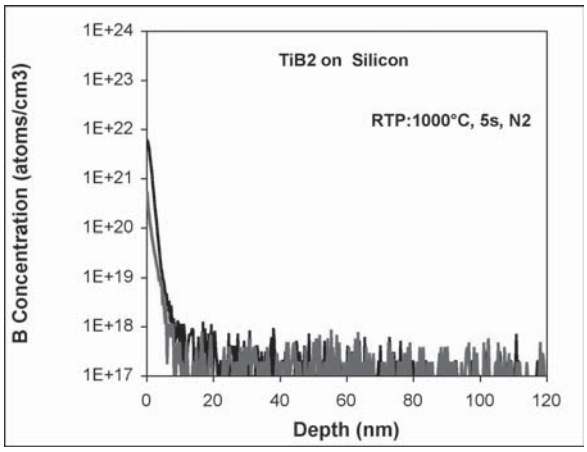

Fig. 7. SIMS depth profiles of B obtained after RTP annealing and after stripping the metal layer prior to the analyses.

based on SIMS results shown in Fig. 7 after TiB_2 annealing at 1000 °C for 5 s. High surface concentrations seen in B profiles could be due to a residual TiB_2 left on the Si surface during incomplete etching prior SIMS analyses. Since the compounds had stoichiometric compositions to ensure thermal stability of dioborides such limited outdiffusion is justified. On the other hand, much lower stability can be observed in boron rich compounds or metal rich borides, which would result in B outdiffusion and silicide formation, respectively. Indeed, we observed such effects in selected deposition processes, which led to clear junction formation with strong diffusion enhancement (not shown here).

To determine barrier heights in a M/S contact system one would use C-V measurements rather than I-V characteristics [33]. In I-V measurements, inhomogeneity of the Schottky barrier, interfacial layer and charges can affect derived barrier heights [34,35]. Ideality coefficient n can be also used as a measure of M/S contact quality such as barrier uniformity, presence of interfacial layer, Fermi level pinning, *etc*. Fig. 8 shows I-V characteristics obtained for TiB_2 on n-type Si after annealing in various thermal conditions. All plots show similar diode behavior, with high barrier heights (ex. 0.96 eV for both 1050 °C/5s and 900 °C/3s). Ideality factor *n* varied

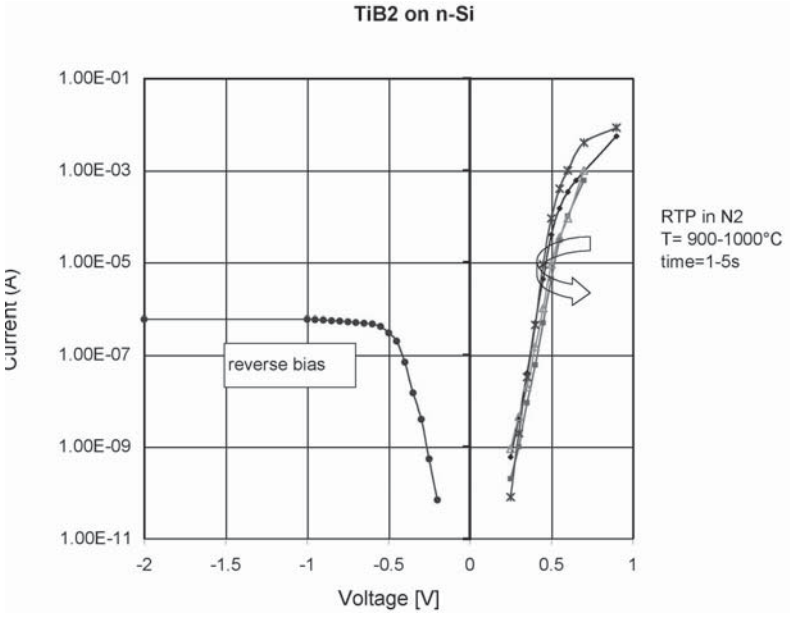

Fig. 8. I-V characteristics for TiB_2 deposited on n-type silicon and annealed in RTP processes at 900-1000 °C for 1-5 sec. The size of the dots was $8 \cdot 10^{-4}$ cm^2.

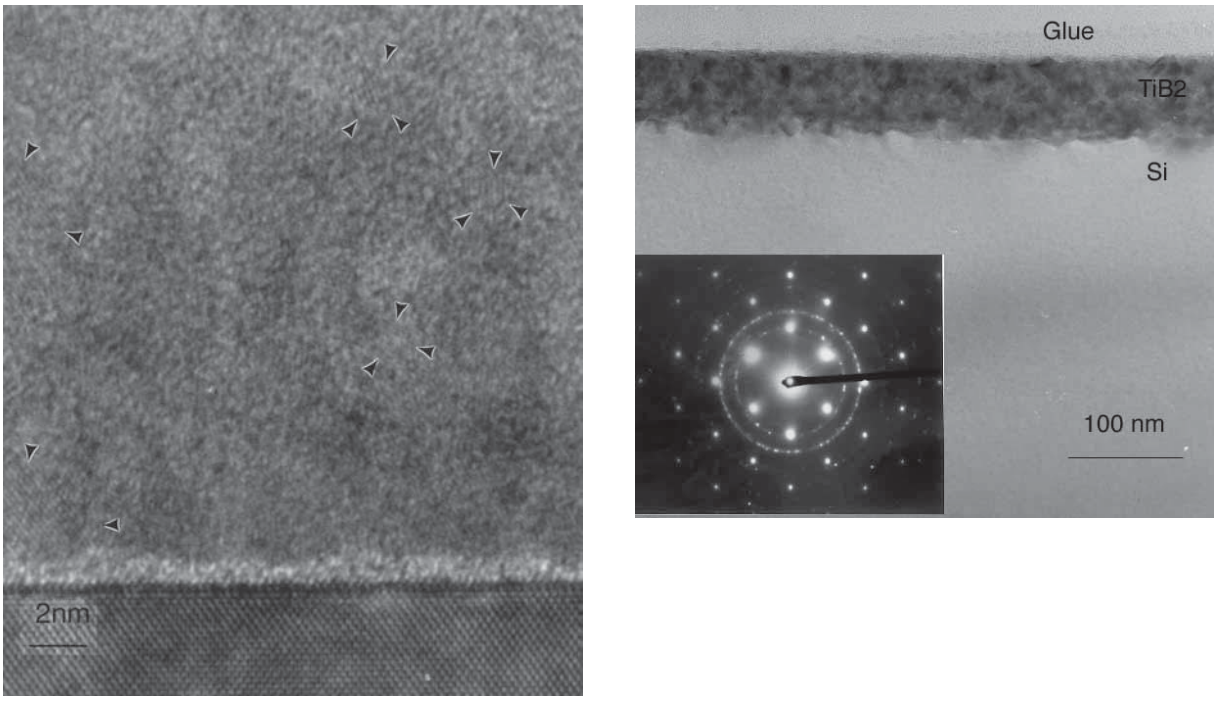

Fig. 9. TEM cross section with diffraction pattern of TiB_2 deposited on Si and annealed at 950 °C for 5 sec, (a), and annealed at 1100 °C for 5 sec. (b). The corresponding as-deposited film was shown in Fig. 1.

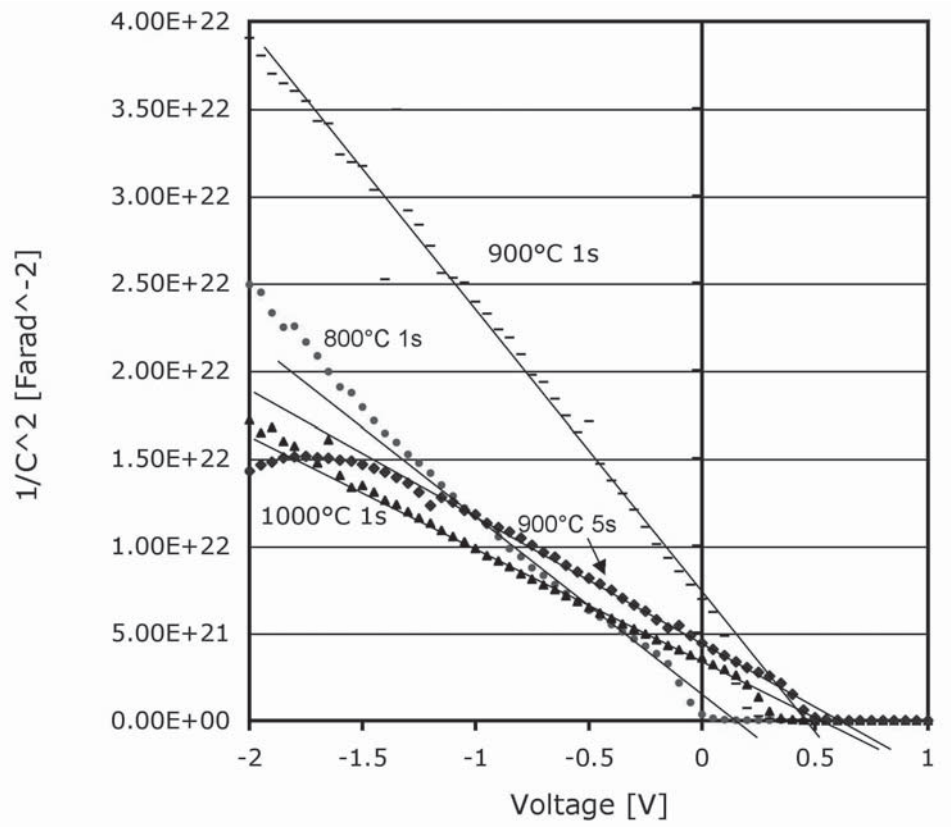

Fig. 10. $1/C^2$ dependence on voltage of TiB_2 contacts annealed at various RTP thermal conditions. Increasing barrier heights are calculated from extrapolation lines.

from 1 as in a perfect Schottky diode to larger values up to 1.3 indicating interface degradation.

TEM cross section (Fig. 9a) illustrates changes in the crystallographic structure within the annealed layers and local interfacial degradation for TiB_2 that can be responsible for the measured I-V characteristics. More pronounced changes are observed at higher temperatures (Fig. 9b) i.e. 1100 °C for 5s, which roughens the interface [36] and results in increased leakage currents. Schottky diode behavior can be analyzed using high frequency C-V characteristics in reverse direction to determine barrier heights. However, the influence of frequency and conductance should be taken into experimental consideration. Capacitance dependence on voltage in Fig. 10 clearly shows changes of the barrier heights that depend on annealing temperatures. Derived values of barrier heights vary from 0.48 eV at very low temperatures to 0.73-0.96 eV at higher temperatures. High thermal stability of these borides may be beneficial in formation Schottky diodes for S/D regions of MOS transistors.

4. CONCLUSIONS

Diborides of Ti, Zr and Hf were tested as contact materials to be integrated with ultra shallow junctions and/or for Schottky diode formation. All borides used in this project showed ohmic behavior on p-type silicon with currents improving by thermal annealing. Sheet resistance and contact resistance values were decreasing with annealing. On n-type silicon, Schottky diodes were formed with high energy barriers. Boron outdiffusion was very limited, if any, for stoichiometric diborides. High temperatures do not lead to decomposition of the borides but cause strong recrystallization.

ACKNOWLEDGMENT

The authors would like to thank International SEMATECH for the support of this work under Project # FEPD005.

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