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APPLICATIONS OF METALLIC BORIDES FOR GATE ELECTRODES IN CMOS INTEGRATED CIRCUITS

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Abstract. We studied the behavior of metallic diborides TiB_2, ZrB_2 and HfB_2 for potential applications as metal gates in Complementary Metal Oxide Semiconductor (CMOS) integrated circuits (IC). The diborides films (20-70 nm) were deposited by e-beam evaporation on thin 20-100 Å thermal oxides. We evaluated work function values of the borides and based on MOS capacitors measurements we found compatibility with p-type Metal Oxide Semiconductor (PMOS) transistors for the annealed gates fabricated with ZrB_2.
Compatibility of these metal gates with the IC processing was tested using rapid thermal processing (RTP) in temperatures of up to 1100 °C. Electrical characterization of the capacitors included capacitance–voltage (C-V), conductance-voltage (G-V), and current-voltage (I-V) measurements. They were complemented by sheet resistance measurements. For material characterization, we used Rutherford Backscattering (RBS), X-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS), cross-section transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) to determine stoichiometry, composition, and crystallographic structure of the processed films as well as possible B outdiffusion. These techniques confirm very high thermal stability of stoichiometric diborides that allows for preserving the sharp interface of metallic gates with the underlying dielectric layer without its degradation during high temperatures RTP. All films undergo recrystallization, detected by XRD as well as by TEM and electron diffraction, which depends on thermal budget of RTP. Decreasing resistivity also results from the grain growth. However, electrical measurements of the test structures after annealing show positive shifts of flatband voltages, which depend on boride type and process conditions.

1. INTRODUCTION

Scaling of metal oxide semiconductor field effect transistors (MOSFET) in CMOS integrated circuits requires significant modification of the gate electrode in sub-90 nm node transistors. Highly doped p+ and n+ polysilicon layers used in PMOS and NMOS transistors, respectively will be replaced by metals to eliminate poly-Si depletion at the interface with dielectric. This effect leads to a decrease of the gate capacitance that for thin gate oxides leads to degradation of device transconductance and limits drive currents. It increases with decreasing gate length due to fringing fields at the gate edges [1,2]. Higher doping levels in poly-Si gates that might alleviate poly-Si depletion are unacceptable due to enhanced dopant (B) outdiffusion into the gate dielectric and channel region [3].

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The new metals should have the same work function Φ_m values as the polysilicon gates and should be equally stable in thermal processing. The requirement of high thermal stability [4] is critical in the gate-first fabrication since high temperatures during source/drain annealing might degrade the metal/dielectric stack via oxidation, recrystallization, reaction with silicon and/or reaction with the new dielectric. In the gate last concept, process integration issues related to deposition/etching and compatibility with the existing layers are more important and very difficult.

A summary of widely studied gate metal candidates both on high *k* dielectric and oxide have been recently published with the emphasis on stability and electrical properties [5,6]. Studies [7] include metal nitrides [8-10] known as effective diffusion barriers, various highly conductive alloys [11] such as Ru and Ru-Ta based materials [12,13], and finally silicides recently introduced for doped polysilicon gates in a self aligned process. Nitrides, as gate materials frequently show a dependence of work function on processing conditions [14]. This may originate from the formation of an interlayer [15] at the interface between the dielectric and metal during thermal annealing and/or from crystallization of the films [16]. It was also postulated that Fermi-level pinning [17-20] might be responsible for such Φ_m changes, which in high *k* dielectrics (but not in SiO_2) can be due to metal induced gap states (MIGS) or intrinsic states in the bandgap. In SiO_2, extrinsic states that are generated by metal-silicon interaction at high *T* annealing, were shown to be responsible for such changes of Φ_m [21-23].

Dual gates for PMOS (~ 5 eV) and NMOS (~ 4 eV) transistors can be obtained using alloys whose composition is specified either during deposition or during annealing of deposited constituent layers. Compositional changes in nitrides due to the N content such as in TiN deposition processes has been used to meet the requirements for tunable gates. Reaction of TaN with C to produce TaCN for PMOS gates and TaSiN [24] for NMOS gates is another option for CMOS metallic gates [25]. Ternary nitrides $Ti_{1-x}Al_xN_y$ (5.1 eV) [26] and $TaSi_xN_y$ were reported as stable up to 950 °C [27]. A newly widely tested approach is fully silicided (FUSI) doped polysilicon [28], which due to dopant segregation at the interface with dielectric allow for tuning work functions to the required values of CMOS [29]. Silicides such as NiSi [30-32] PtSi as well as HfSi [33] have shown compatibility with CMOS technology.

In this work we used diborides known for their superior bulk resistivity (TiB_2 9-15 μΩcm, ZrB_2 7-10 μΩcm and HfB_2 10-12 μΩcm) and high thermal stability. However, reported resistivity for thin films range from 500 μΩcm for as-deposited TiB_2, 250 μΩcm for ZrB_2 to 36 μΩcm for TiB_2 [34] and 25 μΩcm for ZrB_2 [35]. The lowest film resistivity 8 μΩcm was obtained for epi-layers of ZrB_2. Deposition conditions and annealing affect resistivity through crystallographic structure including grain size and porosity, stoichiometry and purity (such as oxygen incorporated during deposition processes).

Stoichiometric diborides are thermally stable [36-39] (ex. 1000 °C 1 hr annealing [40]) with very high melting temperatures. Their thermodynamic stability is comparable or better than that of nitrides or silicides (ex. ΔH [kcal/mol] -77.4 TiB_2, -80.4 TiN, and -32 $TiSi_2$;– 85.6 HfB_2, –54 $HfSi_2$). Self-diffusion of B in TiB_2 is slow at 1000 °C (250 nm in 13 hrs) and increases at 1400 °C and 1600 °C [41] while outdiffusion in RTP [42] is negligible. Less stable metal rich borides form silicides with silicon and diboride at elevated temperatures [43] while boron rich borides release dopant and form stable TiB_2. Work function values for TiB_2 (C-V, Fowler-Nordheim tunneling, contact resistance) show that the work function of CVD deposited layers varies from 4.75 to 5 eV. Borides are very hard and show maximum corrosion resistance. Chemical stability increases from TiB_2 through ZrB_2 to HfB_2. Reported application of TiB_2 was an efficient diffusion barrier for Cu but at lower temperatures [44]. We have also demonstrated excellent thermal stability of a TiB_2 diffusion barrier on Si in RTP [45].

2. EXPERIMENTAL PROCEDURE

Low doped (100) Si wafers both p/p+ and n-type were used for fabrication of capacitors. Thin oxides layers (2 to 10 nm) were fabricated at International SEMATECH using in situ steam generation (ISSG) [46]. Boride layers were deposited by electron beam evaporation at 8 keV from premelted borides chunks. Base pressure in the evaporator was maintained in the high $1 \cdot 10^{-4}$ Pa range and up to $2.5 \cdot 10^{-4}$ Pa during the deposition. Melting point of HfB_2 is the highest of all other borides so the deposition conditions during e-beam evaporation requires the highest power levels. That imposes more stringent requirements for high vacuum to limit contamination levels. The deposited films were 20-70 nm thick. Capacitors with varying area ($3.4 \cdot 10^{-4}$ to $1.8 \cdot 10^{-3}$ cm^2) were patterned using photolithography with wet etching in

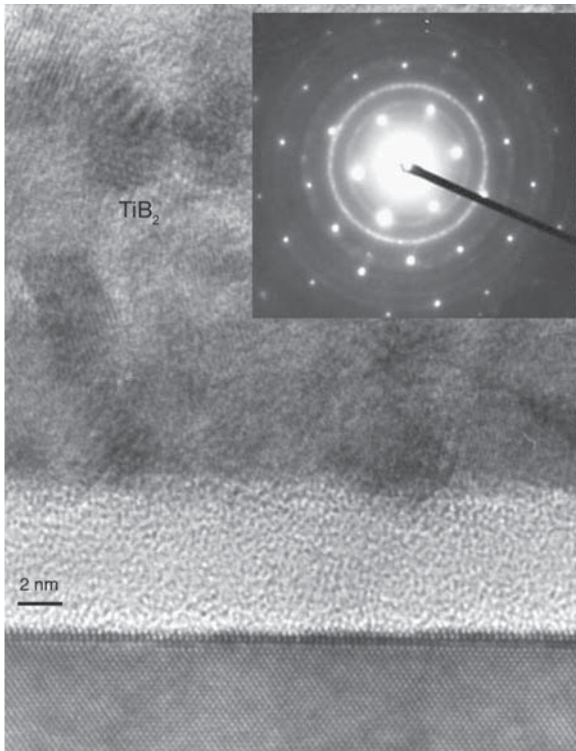

Fig. 1. TEM micrograph and a corresponding diffraction pattern of a TiB_2 layer after annealing at 1100 °C for 1 s.

30% H_2O_2 for TiB_2 and 30% H_2O_2 with 5% HF for ZrB_2 and HfB_2.

Rapid thermal processing at 900 °C-1100 °C for 1-40 sec was performed in an N_2 ambient. Additional forming gas annealing at 400 °C for 30 min was done after RTP steps for selected samples. Ohmic contacts to MOS capacitors were made by striping the backside oxide and by applying an Ag paste. The capacitors were tested before and after RTP using capacitance-voltage, conductance-voltage, and current-voltage measurements. Unpatterned as-deposited and/or annealed layers were tested for sheet resistance and were analyzed by XPS, SIMS, XRD, RBS and cross section TEM.

3. RESULTS AND DISCUSSION

E-beam evaporation results in stoichiometric compositions of diborides as predicted by their respective phase diagrams. This was verified by XPS depth profiling. The layers were metallic, very hard and uniform in thickness with good adhesion to the substrate. Cross section TEM showed that they were amorphous. Resistance of deposited borides films (ex. from 150 μΩcm and 300 μΩcm in the case of TiB_2) decreases (to 50 μΩcm and 180 μΩcm, respectively) during subsequent annealing, but depends strongly on vacuum quality in the e-beam chamber ($7.4\cdot10^{-5}$ Pa and $1.5\cdot10^{-4}$ Pa, respectively) during film deposition. Films deposited at the lowest pressures result in the lowest resistance and show fast decrease of resistivity when annealed in RTP. The lowest resistivity obtained after annealing for ZrB_2 was 66 μΩcm, while for HfB_2 it was 192 μΩcm. For example, RTP decreases the resistance by as much as 3 times for ZrB_2 (from 70 Ω/sq to 25 Ω/sq for 400 Å). Lower resistance indicates higher purity and corresponds to strong recrystallization of the films. We observed borides recrystallization during RTP and a corresponding resistance decrease with no degradation of the gate dielectric (such as stretch-out of a C-V characteristics, leakage currents, or a decreased accumulation capacitance) except for the highest temperatures (1100 °C). Higher thermal budget process leads to larger grain growth as seen in high resolution TEM (HRTEM) and corresponding diffraction patterns. Fig. 1 shows HRTEM cross section of annealed TiB_2 (1100 °C, 1 s) with large grain growth and a smooth interface with oxide. Oxide thickness remained the same as deposited (not shown here). We confirmed diborides formation by identifying small spot diffraction patterns. Hexagonal TiB_2 was identified by the following lattice constants a=3.038 Å and c =3.27 Å. Within the films, there is no preferential orientation of the grains or nonuniformity in the grain distribution. Both XPS and RBS results also show good stability of deposited films in RTP.

Grain growth can be related to the work function modification caused by orientation effects [47] as seen in high-resolution work function measurements in single grains using the Kelvin probe microscope [48]. Work function anisotropy causes unpredictability of the work function in processed devices. It originates in deposition [49], where various techniques [50] (physical vapor deposition, chemical vapor deposition, atomic layer deposition, *etc.*) or even only various process conditions [4] (rate, *etc.*) used for the same material result in different properties. Variations in work function values related to crystallographic orientations predicted theoretically and verified experimentally [51] can be as large as 1 eV [52,53]. A contribution from a thin nanometer layer can change the work function [54] so the reaction at the metal-oxide interface of the device can indeed change the device operation.

C-V measurements were performed at 1MHz, 100 Hz, and 10 Hz using a parallel conductance/

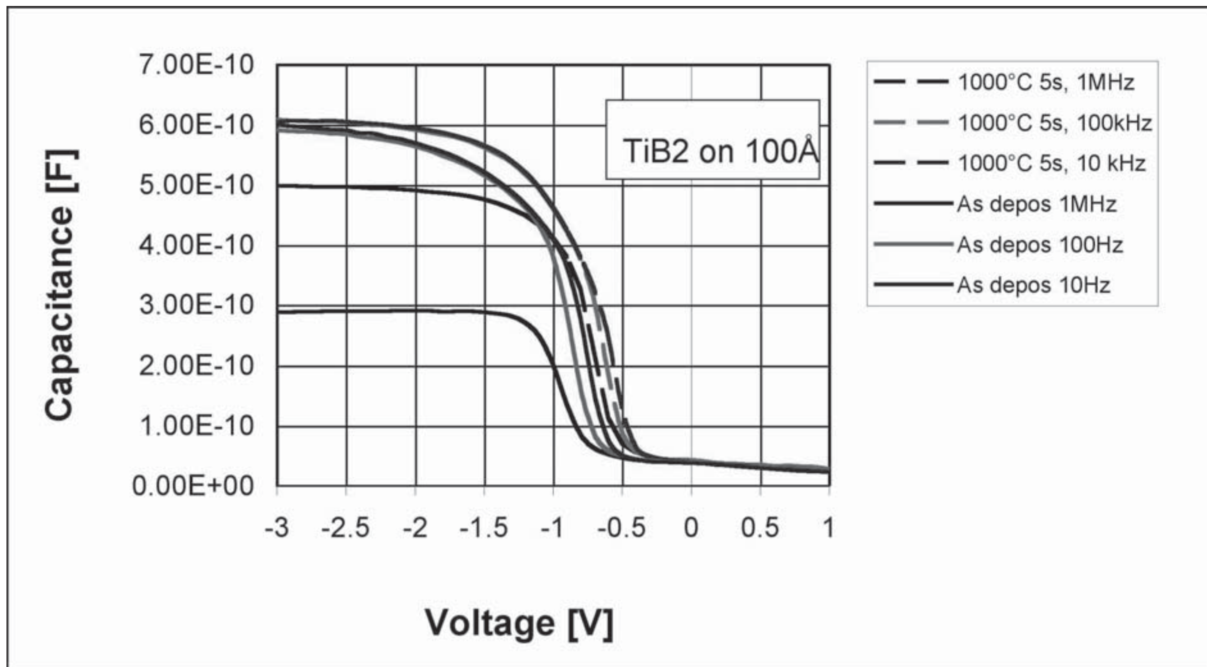

Fig. 2. C-V characteristics for TiB_2 gates obtained before and after annealing at 1000 °C for 5 s. Both high and low frequencies were used in the measurements.

capacitance model. Fig. 2 shows C-V results for TiB_2, where the frequency dispersion in accumulation capacitance indicates parasitic series resistance while frequency influence in the V_{FB} shift indicates the presence of interface traps. Annealing reduces the resistance (seen as a difference in 1MHz plots before and after annealing compared with the low frequency plots) but the oxide thickness does not change as seen by constant accumulation capacitance at low frequencies. That means that there is no interlayer formation at the metal-oxide interface that would lead to dielectric formation. However, there is a positive shift in the flatband voltage of about 0.2 V that may indicate a work function change, or a decrease in a positive charge, and/or B diffusion due to annealing. Since a similar shift of 0.2 eV was seen by Kelvin probe for TiB_2 it appears to be related to the work function change. Similar behavior was observed for other borides where C-V shifts were obtained; however, these changes were larger than for TiB_2. Fig. 3 illustrates such a behavior for ZrB_2 where a V_{FB} determined for equivalent oxide thickness (EOT) results in Φ_m varying from 4.38 eV to 4.85 eV after annealing at 1000 °C. This shift was very reproducible for ZrB_2 gates deposited on p-type Si in several processes and did not depend on oxide thickness. An increase in the barrier height due to annealing is confirmed by Fowler-Nordheim tunneling (F-N) [55,56] for deposited and annealed samples using RTP 1000 °C 10 s (Fig. 4). Decreasing injection current from the gate in the annealed samples indicates that the barrier height at the metal-oxide interface increases due to annealing. Similar effects

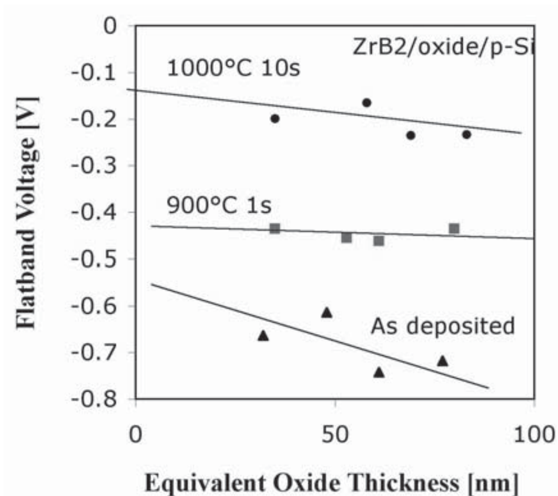

Fig. 3. Flatband voltage dependence on effective oxide thickness for ZrB_2 electrodes obtained before and after annealing in RTP.

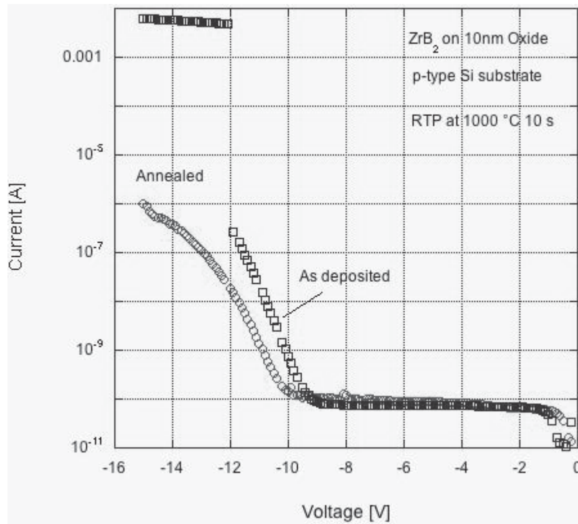

Fig. 4. F-N characteristics obtained for ZrB_2 gates before and after annealing in RTP.

of work function changes were also observed for nitride gates [57-59]. We used the determined work function values to simulate C-V characteristics of a capacitor with a ZrB_2 gate using quantum mechanical effects (NIST program). The results of theoretical calculation are shown in Fig. 5 together with experimental results obtained using ZrB_2 as an electrode.

It is important to monitor the stability of metal gates at high temperatures as it may lead to oxide degradation. From the conductance measurements (corrected for series resistance to better present the interface traps) shown in Fig. 6, we can conclude that the diborides do not contribute to trap generation during annealing as seen in a decreased

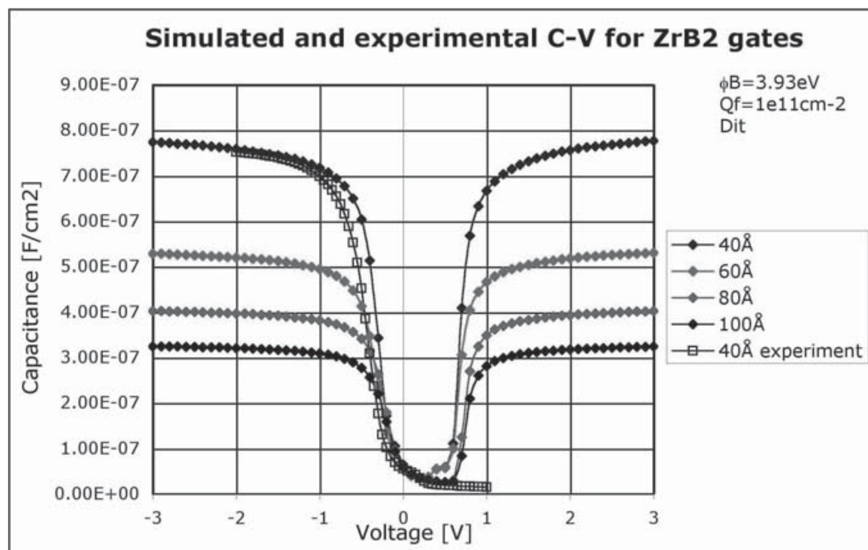

Fig. 5. Comparison of C-V characteristics simulated using barrier height of 3.93 eV and experimentally obtained for ZrB_2 electrodes.

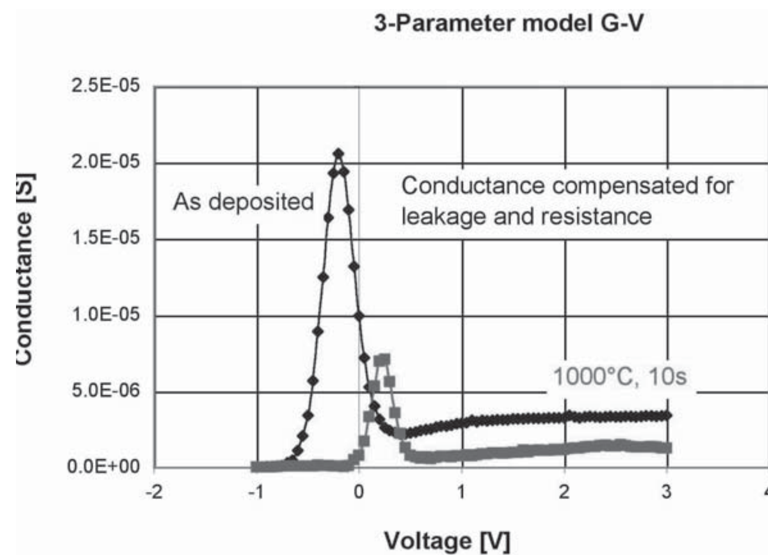

Fig. 6. Conductance-voltage characteristics obtained for ZrB_2 before and after RTP annealing.

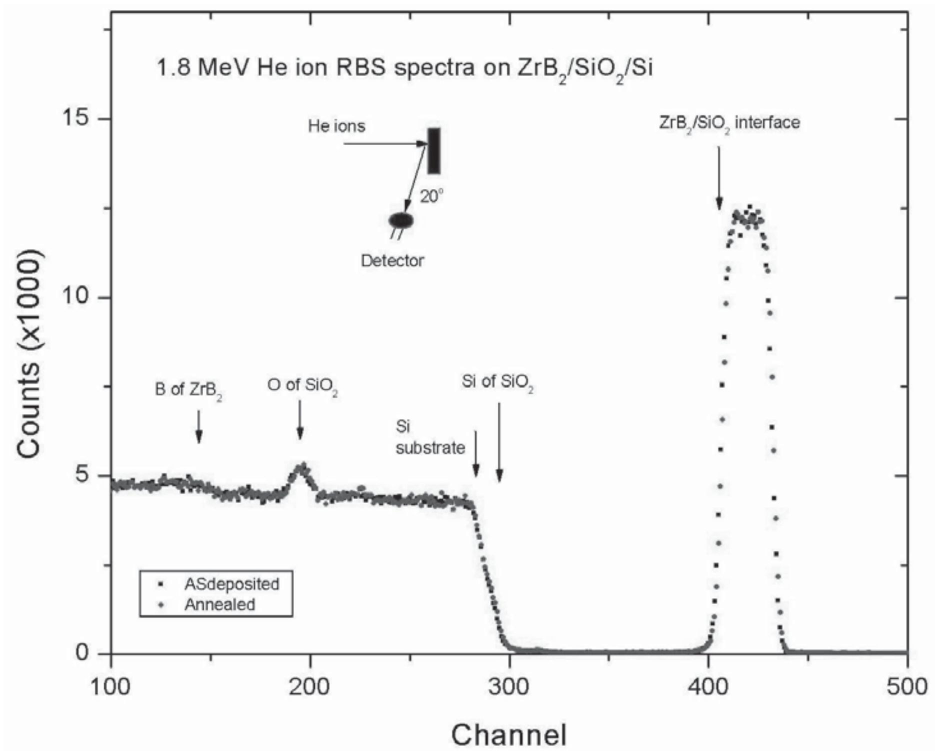

Fig. 7. RBS spectra for ZrB_2 deposited on 80 Å oxide and annealed in RTP.

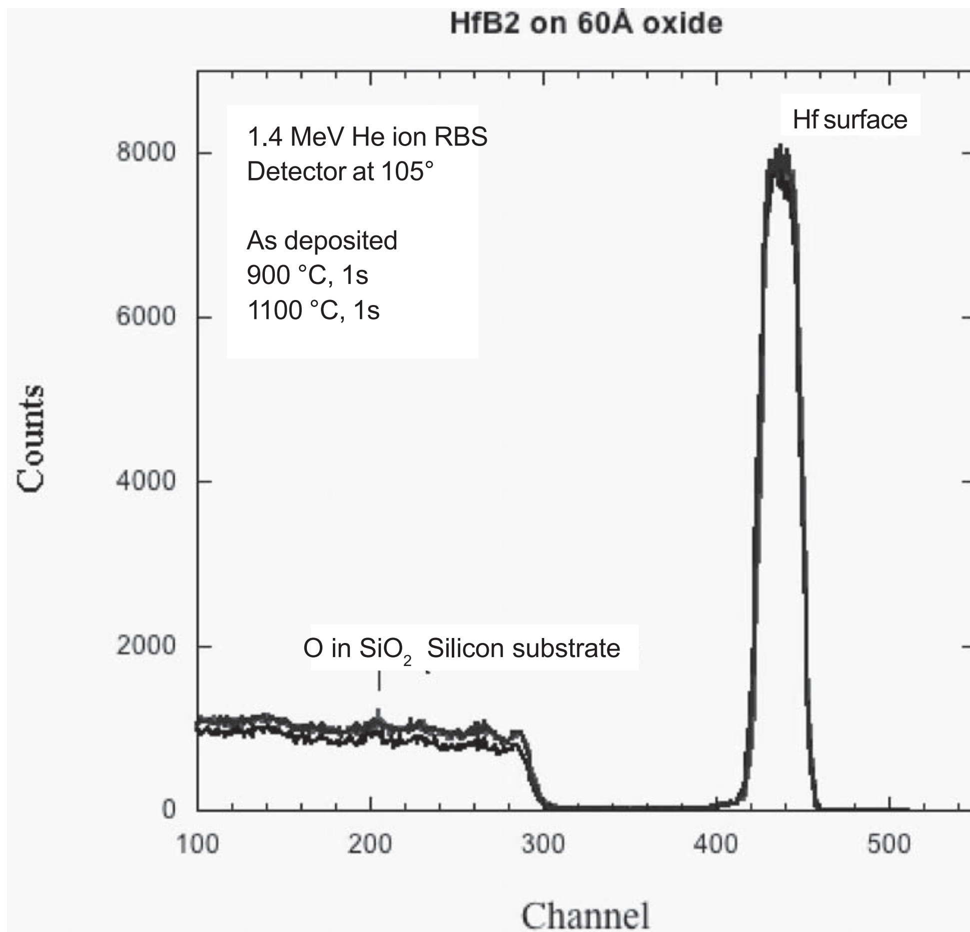

Fig. 8. RBS spectra for HfB_2 deposited on 60 Å oxide and annealed in RTP using various thermal conditions.

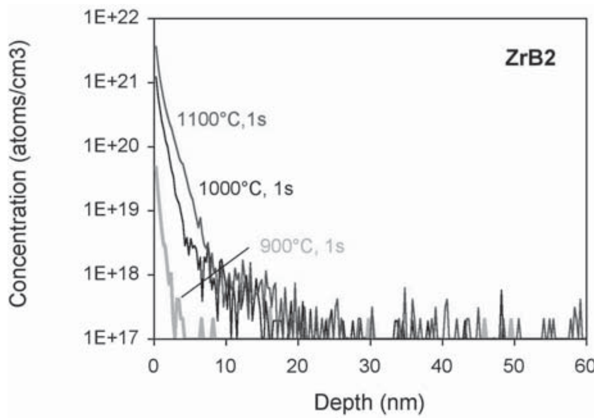

Fig. 9. SIMS depth profiles of B obtained after annealing of ZrB_2 in RTP.

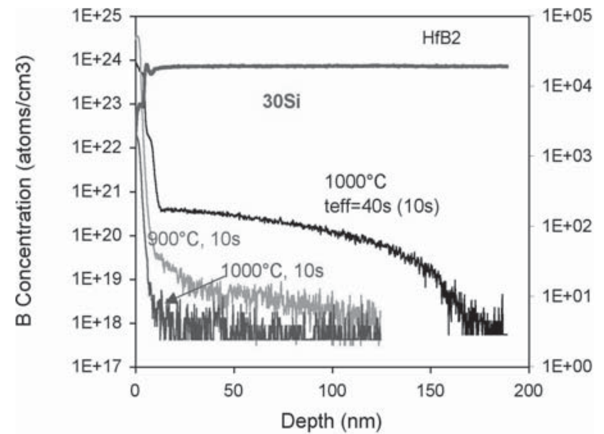

Fig. 10. SIMS depth profiles for HfB_2 gates obtained after RTP.

conductance peak within the depletion. A shift in G-V characteristics reproduces the shift in the flatband voltage in C-V characteristics due to RTP annealing.

Stability of MeB_2 was verified in experiments using films of various thicknesses and processed in various thermal conditions. Our results confirm the uniformity of the layer composition and structure both in the bulk and at the interface with the dielectric. RBS spectra (Fig. 7) obtained for ZrB_2 show no changes in composition and layer thickness processed at 1000 °C for 10 s. Very similar results were also obtained for other borides: TiB_2 and HfB_2 (Fig. 8). Low angle of the beam detection was used to ensure high depth resolution in each case.

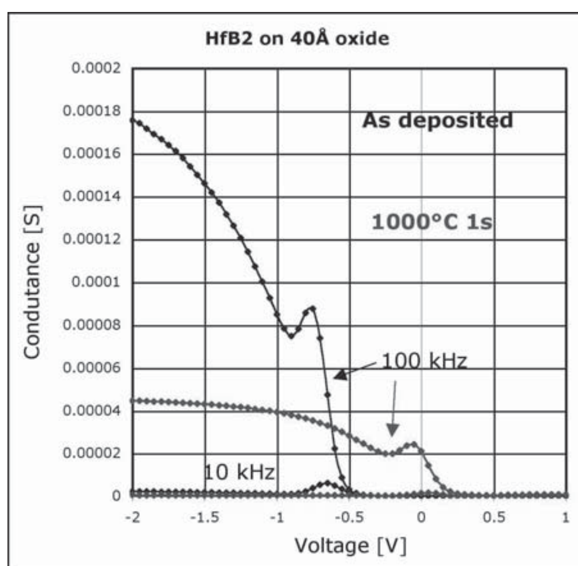

Fig. 11. Conductance results for HfB_2 as deposited on 40 Å oxide and annealed (w/o resistance corrections).

Since borides were used as gate electrodes, we monitored plausible B outdiffusion that might occur should compound decomposition take place. Stoichiometric diborides MeB_2 [60] have high thermodynamic stability and very low diffusivity of B $\approx 10^{-17}$ cm^2/s at 1000 °C [41]. Nonstoichiometric borides, on the other hand, such as boron rich or titanium rich ones are much less stable. Reactions leading to stable MeB_2 with simultaneous B diffusion (in B rich films) or silicide formation (in Me rich films) have been observed [61] in annealing at 1000 °C for 1 hr. If outdiffusion of B occurs, degradation of the dielectrics [62] would follow with possible channel doping. An example of B profiles is shown Fig. 9 after ZrB_2 annealing and chemical stripping of the ZrB_2 layer before SIMS profiling. These profiles are possibly due to a residual ZrB_2 left on the surface after etching rather than a real B outdiffusion in the RTP conditions used. Similar results were obtained also for TiB_2 (not shown here). However, the stability is not unlimited and a sharp increase in the thermal budget (1000 °C 40 s) leads to B outdiffusion into Si. This is shown for HfB_2, where the stability shows degradation for high thermal budget RTP (Fig. 10) and very large B outdiffuion is detected. That may be caused by undetected nonstoichiometry, which could be related to difficult deposition conditions of HfB_2 due to its highest melting point compared to other studied diborides.

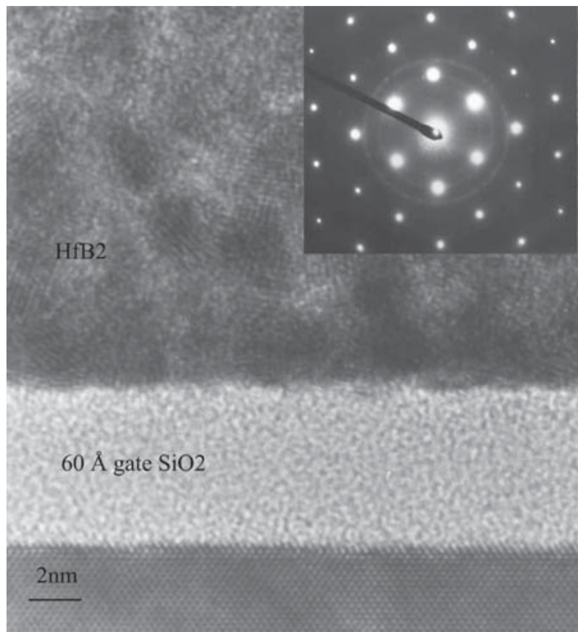

Fig. 12. TEM cross section at high resolution and diffraction pattern obtained for HfB_2 on 60 Å oxide after RTP.

Electrical measurements of HfB_2 show positive voltage shifts in C-V and in G-V characteristics that are larger than those for TiB_2 and ZrB_2. However, there is no degradation in accumulation capacitance, indicating unchanged oxide thickness and no interface trap generation. A decrease of resistance is also seen in the conductance measurements (Fig. 11), which decreases in the accumulation range (i.e. at negative voltages) and show a decrease in the peak related to the interface traps. Leakage does not increase due to annealing.

Recrystallization of the HfB_2 films is very fast as seen in Fig. 12. A Cross section TEM micrograph shows a polycrystalline structure within a HfB_2 layer annealed at 1000 °C for 1s. SAED pattern confirms hexagonal structure of HfB_2 with lattice constants of a = 3.13 Å and c = 3.48 Å. The thickness of the oxide is the same as after deposition and surface roughness is not degraded by the grain penetration.

4. SUMMARY

MOS capacitors with gate electrodes made of diborides were tested for compatibility with the ITRS requirements for work function in PMOS transistors and for process integration constrains. Diborides deposited by e-beam evaporations result in stoichiometric composition, which ensures their thermal stability in subsequent thermal processes. Diborides are susceptible to oxidation during thermal processing so a neutral gas ambient should be used. There is no interfacial reaction with the oxide that would lead to changes of dielectric thickness. Strong recrystallization of the films was observed for all borides without damaging the interface with the gate oxide. A sharp decrease in the resistivity values during annealing is related to deposition and annealing conditions. A change in the effective work function is observed for all borides due to annealing.

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